Universal ByteBlaster

Hardware Manual

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Revision 1.1

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1 About this Document

1.1 Purpose

This document describes Hardware installation, features, specification and operation for AMFELTEC Universal ByteBlaster device.

1.2 Feedback

AMFELTEC makes every effort to ensure that the information contained in this document is accurate and complete at time of release. Please contact AMFELTEC if you find any errors, inconsistence or have trouble understanding any part of this document.

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Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	May 20, 2005
1.1	Minor changes	June 20, 2005

2 General Description

2.1 Introduction

The Universal ByteBlaster is the hardware interface converter of a standard parallel port to the 10 pin on test board connector. The ByteBlaster provides electrical conversion of the signals between 5V logic level of the parallel port and multi-voltage signal level used on the different CPLDs and FPGAs.

Figure 1: Universal ByteBlaster

The Universal ByteBlaster can be setup for different mode of operation. Appendix B shows setting for the SW3 switch that defines ByteBlaster operation mode.

In the test mode the internal logic of the ByteBlaster can be updated from the PC by using iMPACT program from Xilinx Corp.

3 Features

- Cost effective replacement for the multiple ByteBlasters from the different FPGA vendors
- Allows performing ByteBlaster functionality for the different FPGA/CPLD vendors. (define by switch) like ALTERA, XILINX, LATTICE, ATMEL
- Allows performing I2C master operation
- Supports operation while power up with any voltage from 1.2 V to 5.5 V
- Interface with standard 25-pin parallel port on PCs
- Flexible design and full schematic allows customers to modify internal logic for correction or for implementing new futures

3.1 Connections

The 25-pin male header connects to a parallel port PC with a standard parallel cable. The 10 pin male connector via cable connects to the test board. The target board must provide power and ground to the ByteBlaster. The power for the ByteBlaster has to be the same as the I/O power for programmable device (devices) and has to be from 1.2Volts up to 5.5Volts. Examples connection between Universal ByteBlaster and test board shows in Appendix A.

4 Appendix A: JTAG Programming Interface

Function	eX10 (2x5) connector (J5)	XILINX FPGA HEADER
VCC (5v- 1.2V)	4	1
TDO	3	4 (D / P)
TDI	9	5 (DIN)
TMS	5	6(PROG)
TCK	1	3(CCLK)
GND	2,10	2

Table 1: JTAG Programming Interface for XILINX

Function	eX10 (2x5) connector (J5)	2x5 Altera connector
VCC (5v- 1.2V)	4	4
TDO	3	3
TDI	9	9
TMS	5	5
TCK	1	1
GND	2,10	2,10

Table 2: JTAG Programming Interface for ALTERA

Function	eX10 (2x5) connector (J5)	1x8 Lattice Download Cable header	1x10 Lattice SPI Flash Programming header
VCC (5v- 1.2V)	4	1	1
TDO	3	2	2(SFLASH_Q)
TDI	9	3	3(SFLASH_D)
TMS	5	6	nc
TCK	1	8	8(SFLASH_C)
ISPEN/BSCAN	8	nc	4(SFLASH_S_N)
RESET	6	nc	nc
GND	2,10	7	7

Table 3: JTAG Programming Interface for LATTICE

Function	eX10 (2x5) connector (J5)	TBD
VCC (5v- 1.2V)	4	TBD
TDO	3	TBD
TDI	9	TBD
TMS	5	TBD
TCK	1	TBD
INI	6	TBD
AF	8	TBD
GND	2,10	TBD

Table 4: JTAG Programming Interface for ATMEL

5 Appendix B: Operation Modes

The following table shows different operation modes depending of DIP Switch setting:

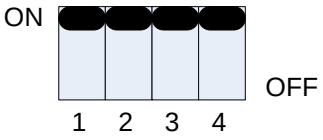
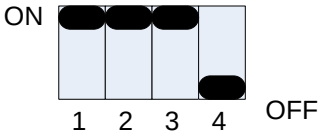
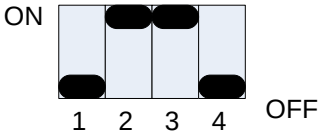
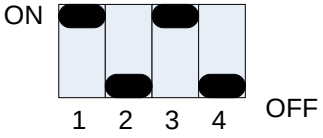
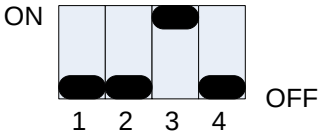
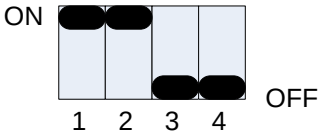
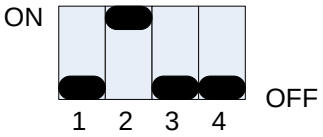
	**Update logic mode.**
	**Xilinx JTAG interface mode.**
	**Altera JTAG interface mode.**
	**Lattice JTAG interface mode.**
	**ATMEL JTAG interface mode.**
	**SPI interface mode.**
	**I2C JTAG interface mode.**

Table 5: Operation Modes

6 Appendix C: Limited Warranty

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