PCI Express Extender

Hardware Manual

July 23, 2008
Revision 1.4

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1 About this Document

1.1 Purpose

This document describes Hardware installation, features, specification and operation for AMFELTEC PCI Express Extender.

1.2 Feedback

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To provide your feedback, please send an email to support @amfeltec.com

Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	01-05-2008
1.4	Minor changes	09-01-2008

2 General Description

2.1 Introduction

The PCI Express Extender is a extender for x1 link PCI express bus with integrated logic to support debugging and verification of PCI express cards (referred as UUT, Units-Under-Test). The UUT is plugged-in to the motherboard slot through the extender.

The extender uses a bus switch to connect/disconnect the UUT PCI express card from the motherboard without shutting down the system. This flexibility minimizes the testing time and protects the motherboard from damage such as overcurrent

The extender supports two ways of feeding the secondary PCI express bus with power: internally, through the motherboard PCI express slot (+3.3V and +12V), and from an external power supply. The external power supply has to provide +5V and +12V voltages to satisfy all PCI express needs:

+12V and 3.3V

The extender fully protects your UUT and host system from damage by monitoring and limiting the voltage and current.

The extender includes logic (based on the Xilinx CPLD XC9536XL-10) for debugging and verification purposes:

- FPGA ByteBlaster functionality for the different types of the FPGA (like Xilinx, Altera, Atmel, Lattice) through the external cable
- Master I2C and SPI interfaces

The CPLD logic can be customized as required. The standard package of the extender includes full schematics and logic for the CPLD.

All these functions communicate with the computer through a parallel interface. The same interface can be used to update or to load the customer's specific functions into the on- board CPLD.

The extender supports two types of the computer enclosures: the 2U and the standard profiles. The angled connector of the extender allows for easy access to the UUT card.

The Extender has additional support tabs for the stabilization of the PCI express add-in card (UUT). Amfeltec Corporation filed a Patent Application that covers this unique future.

Figure 1: PCI Express Extender

3 Specifications/Features

3.1 Power and Signaling

- Visualization of UUT powers +3.3VAUX, +3.3Volt and +12V (Green LEDs).
- Overloading Protection (OLP) on the UUT +3.3V and +12V supplies.
- Under-voltage protection (UVP) on the UUT +3.3V, +12V.
- UUT power failure protection (in case OLP or UVP and indication filer on the LED (red).
- Extender can be powered from primary PCI express or from external power supply (defined by Jumpers block, can be used on any computer power supply with standard IDE interface power connector).
- Meets PCI express 1.1 specification.
- Support programmable equalization, amplification and de-emphasis via on board resistor.
- Supports live insertion for plug-in card.

3.2 Logic

- Supports ByteBlaster functionality for different FPGAs: Xilinx, Altera, Lattice
- Converts parallel interface signals to/from I2C or SPI bus signals
- Supports operation while power up with any voltages from 1.2V – 5.5 V

3.3 Debugging Support

- Includes 2 brackets to support normal and 2U computer boxes
- Allows access to the PCI express JTAG interface of the UUT

3.4 Software

- Hot swapping software for saving and restoring PCI configuration for UUT for hot-swap operation (refer to *eX10 Software Manual for more details*)
- I2C master write/read software
- Supported operating systems: Windows, Linux FreeBSD

3.5 Power Limits

Power	Threshold for under voltage monitoring	Maximum current for Over voltage protection	Comments
+3.3V	+2.78V min.	3.0 A	
+3.3V Auxiliary	+2.78 V min	470 mA	
+12V	+10.5V min.	5.5 A	

Table 1: Power Limits

4 Hardware Description

4.1 Board Layout

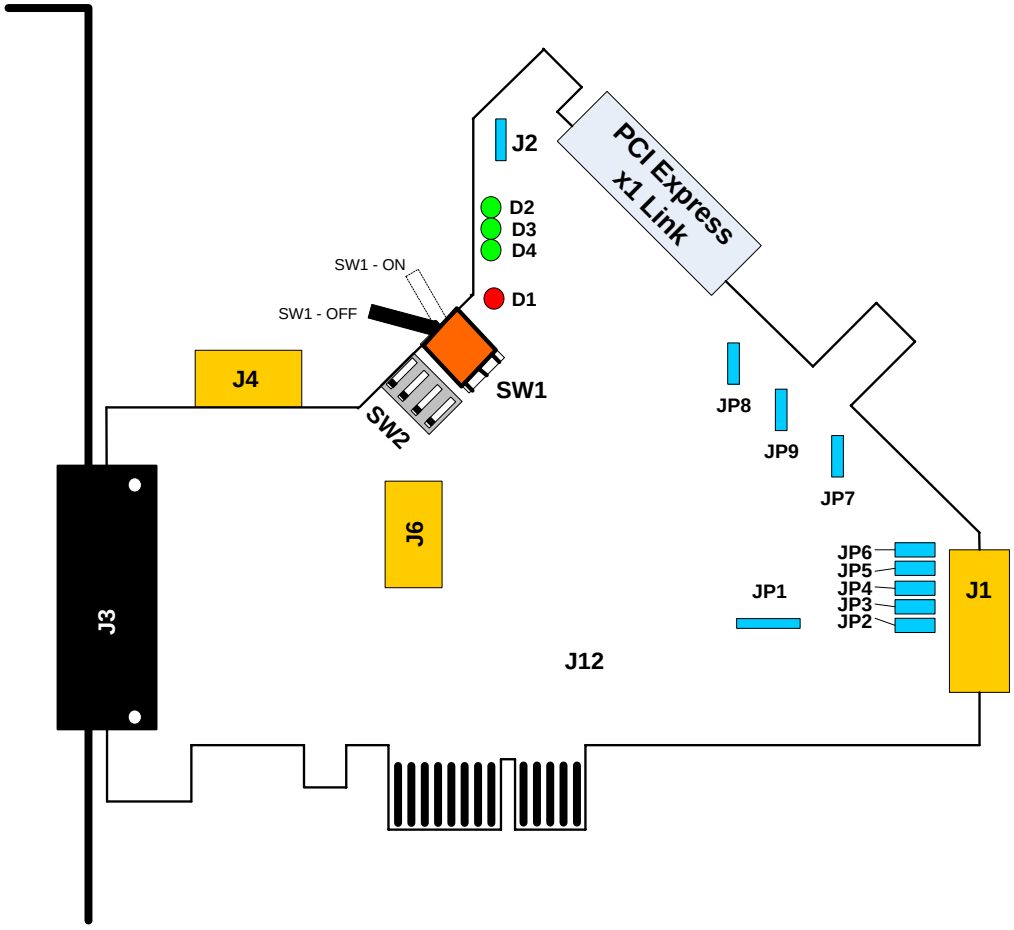


Figure 2: Board Layout

4.2 LEDs

Name	RefDes	Color	Usage
+3.3 Volt	D3	Green	3.3Volt power on the UUT
+3.3 V AUX	D2	Green	3.3 Volt local Auxiliary Power
+ 12 Volt	D4	Green	+12Volt power on the UUT
Power Fail	D1	Red	UUT power Fail (In case overload or under voltage)

Table 2: LEDs

In case that “Power Fail” LED is ON (overload or under voltage condition happens) it is necessarily to toggle on UUT power switch SW1 for reset fail condition.

4.3 Switch

Name	RefDes	Type	Usage
UUT Power ON/OFF	SW1	Toggle x 1	Power switch for the UUT. In case Power OFF – all PCI signals from the Primary PCI bus are disconnected from the UUT (Hot swapping)
MODE	SW2	Toggle x 4	Four toggle switches define extender logic between Parallel interface and UUT download interface

Table 3: Switches

Follow table shows setting for the different SW2 switch settings:

1	2	3	4	*Usage*
ON	ON	ON	ON	Test mode for update CPLD logic itself (XC9572XL-10VQ44)
ON	ON	ON	OFF	JTAG / Parallel download interface for Xilinx
OFF	ON	ON	OFF	JTAG / Parallel download interface for Altera
ON	OFF	ON	OFF	JTAG / Parallel download interface for Lattice
OFF	OFF	ON	OFF	Download interface for ATMEL
ON	ON	OFF	OFF	Master SPI interface
OFF	ON	OFF	OFF	Master I2C interface
ON	OFF	OFF	OFF	SPARE mode
OFF	OFF	OFF	OFF	SPARE mode

Table 4: Switch SW2

4.4 Jumpers

RefDes	Type	Usage
J2	3 pins jumper	Ground pins for the Test Equipment connection
JP7	2 pins jumper	Disable Auxiliary Power.
JP8	2 pins jumper	Overset PRSNT signal from the secondary PCI express bus.
JP9	2 pins jumper	Set mask for the Power On SW1 status and for JP7
JP11	3 pins jumper	Define power source for the Auxiliary power. If 1-2 pins close, then power taken from primary PCI express bus. If 2-3 pins are closed, then power will be taken from the internal 3.3V power.
JP2,JP3, JP4,JP5,JP6	Block of Jumpers (5x3)	Define power source for the UUT bus. If 1-2 pins on the all jumpers are close, then extender logic and UUT will be powered from Primary PCI express bus. If 2-3 pins on all jumpers are closed, then extender and UUT will be powered from External Power supply

Table 5: Jumpers

4.5 Connectors

RefDes	Type	Usage
J4	5x2 (2.5 mm) header	ByteBlaster connector
J3	DB-25 (male)	Parallel port connector for communication with main computer
J6	5x2 (2.5 mm) header	JTAG connector.
U11	1x PCI express female connector	Secondary PCI express connector for add-in card.
J1	Disk drive power connector	External Power supply connector

J5	1x PCI express male connector	Primary PCI express connector for plug-in extender to the motherboard.

Table 6: Connectors

5 Installation

5.1 Hardware Installation

- To install the PCI express extender power off the host computer. The shipped package includes two types of brackets: low and high profile. If you like to change the brackets, you need to unscrew the installed bracket from the connector J3 and replace by another bracket.
- The Extender is a universal solution for debugging different types of PCI express devices. In order to properly configure the extender, please refer to Table 4.
- The extender has integrated Universal ByteBlaster. If you are going to use ByteBlaster, please refer to Table 3 or Appendix B (switch SW2) to set the correct mode of operation.
- Select power source for UUT. The extender provides two options for selecting proper power source: internal power from the primary PCI bus and external power supply. In order to select the power source, refer to Table 4 .
- Install the extender into a PCI express slot. Extender can be installed in any PCI express connector (1x/4x/8x/16x links). **Important Note: Secure the extender using a screw in the metal bracket!**
- Install UUT board into extender.
- In case you are using external power supply you have to turn it on **first** (before powering up the computer). Then, set switch SW1 to position ON (enable power) for secondary PCI bus and UUT.

Now, you can power-up the host computer.

BE SURE THAT THREE GREEN LEDS (D2, D3 and D4) ARE ON!

In case led D1 is red, please turn off your computer and check the extender configuration jumpers or UUT device for power shortage.

5.2 Software Installation

For normal operation, you don't need to install additional software. But if are going to use HOT-SWAP functionality, you need to install eX10Suite Software Suite (refer to ex10Suite Software Manual for more details).

6 Hot-Swap Support

Perform hot swapping with a certain degree of carefulness. Remember that PCI configuration won't be loaded or automatically updated on insertion of a new UUT device unless you use the supplied HOT SWAP software to reload the UUT's PCI configuration.

6.1 Remove UUT Device

The following steps describe detail sequence for removing UUT device:

1. Save UUT PCI configuration into a file (refer to Software Manual for *more details).*
2. Unload all device drivers associated with the UUT.
3. Set the switch SW1 to "OFF" (disable power).
4. Now, you can remove UUT device from the secondary PCI Express connector.

6.2 Install UUT Device

The following steps describe details sequence for installing UUT device back to the system:

1. Plug in UUT device into the secondary PCI express connector.
2. Set the switch SW1 to "ON" (enable power).
3. Restore PCI configuration for the UUT device.
4. Now, the UUT device is ready for use.

7 Appendix A: JTAG Programming Interface

Function	Extender (2x5) connector (J4)	XILINX FPGA HEADER
VCC (5v- 1.2V)	4	1
TDO	3	4 (D / P)
TDI	9	5 (DIN)
TMS	5	6(PROG)
TCK	1	3(CCLK)
GND	2,10	2

Table 7: JTAG Programming Interface for XILINX

Function	Extender (2x5) connector (J4)	2x5 Altera connector
VCC (5v- 1.2V)	4	4
TDO	3	3
TDI	9	9
TMS	5	5
TCK	1	1
GND	2,10	2,10

Table 8: JTAG Programming Interface for ALTERA

Function	Extender (2x5) connector (J4)	1x8 Lattice Download Cable header	1x10 Lattice SPI Flash Programming header
VCC (5v- 1.2V)	4	1	1

TDO	3	2	2(SFLASH_Q)
TDI	9	3	3(SFLASH_D)
TMS	5	6	Nc
TCK	1	8	8(SFLASH_C)
ISPEN/BSCAN	8	nc	4(SFLASH_S_N)
RESET	6	nc	Nc
GND	2,10	7	7

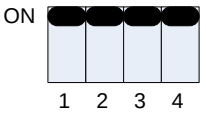
Table 9: JTAG Programming Interface for LATTICE

Function	Extender (2x5) connector (J4)	TBD
VCC (5v- 1.2V)	4	TBD
TDO	3	TBD
TDI	9	TBD
TMS	5	TBD
TCK	1	TBD
INI	6	TBD
AF	8	TBD
GND	2,10	TBD

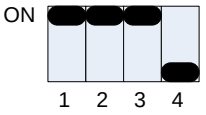
Table 10: JTAG Programming Interface for ATMEL

8 Appendix B: Operation Modes

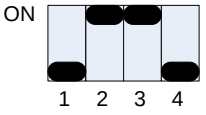
The following table shows different operation modes depending of DIP switch setting:



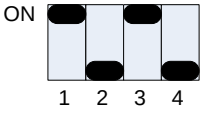
Update logic mode.



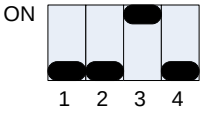
Xilinx JTAG interface mode.



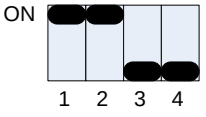
Altera JTAG interface mode.



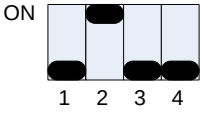
Lattice JTAG interface mode.



ATMEL JTAG interface mode.



SPI interface mode.



I2C JTAG interface mode.

9 Appendix C: Limited Warranty

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