PCI Test Backplane

Hardware Manual

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Amfeltec Corp.
3-1136 Center Street, Suite 402
Thornhill, ON L4J 7B1

www.amfeltec.com

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1 About this Document

1.1 Purpose

This document describes the hardware installation, features, specification and operation of the AMFELTEC PCI Test Backplane.

1.2 Feedback

AMFELTEC Corp. makes every effort to ensure that the information contained in this document is accurate and complete at time of release. Please contact AMFELTEC Corp. if you find any errors, inconsistence or have trouble understanding any part of this document.

To provide your feedback, please send an email to support@amfeltec.com

Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	September 15, 2008
1.1	Minor changes	November 10, 2010
1.2	Minor changes	January 28, 2013

2 General Description

2.1 Introduction

The “PCI Test Backplane” (backplane) is a four slot 32-bit PCI backplane that connects to the upstream host computer via two cables (standard CAT6 and 10 wires flat cables) and x1 PCI express Host Card. The Host Card has to be plugged into the PCI express connector on the motherboard of the upstream host computer. The Backplane supports debugging, verification as well as production testing and programming of PCI based cards. Using PCI Test Backplane eliminates the risk of damage to the host computer during debugging, programming and testing PCI cards and at the same time the host computer can be removed from the testing area to free up space.

By using bus switches the four 32-bit PCI connectors can be connected / disconnected from the PCI express upstream link without shutting down the host system. This allows easy replacement of plugged in PCI cards (referred UUT, Unit-Under-Test) on the backplane and significantly decreases testing/verification time.

All four 32-bit PCI connectors are powered from separate power controllers. Those power controllers are independent and have over current protection and under voltage protection. Thus all UUTs and host system are fully protected from damage in case of power shortage. Each slot has additional auxiliary power connector (GND, +12 Volts and +5 Volts) to provide per slot power to the external devices (UUTs) connected to the test backplane.

The PCI Test Backplane has four connectors (one for each PCI slot) to provide access from an external programmer/emulator to the PCI bus JTAG signals. This feature is unique and not found on other PCI backplanes or motherboards. It gives the possibility to run JTAG production tests, use a JTAG emulator for UUT debugging and/or to use **“eLoader”™** from AMFETLEC Corp. for programming/loading CPLD/FPGA on the UUT during debugging or production cycle.

The backplane has surface-mount LEDs which provide a convenient visual check for the main power status (+12V, +5V, -12V, +3.3V, +5VSB), power controller status per PCI slot (power ON/OFF, power GOOD/FAIL) and the upstream PCI express connection status.

An additional PCI Test Backplane has a debug connector with all PCI signals easily accessible for probing or connecting to a logic analyzer.

2.2 Package Details

The PCI Test Backplane includes following components:

1. PCI Test Backplane (Figure 1)
2. PCI express Host Card (Figure 2)
3. Data CAT6 cable and control flat cable (both cables 7 ft.)

4. User manual

Figure 1: PCI Test Backplane

Figure 2: PCI express Host Card

3 Requirements/Features

3.1 Power/Interface Signals

- Visualization of UUT power status +3.3VAUX, +3.3Volt and +12V (Green LEDs)
- Overloading Protection (OLP) on the UUT +3.3V, +5V and +12V supplies
- Under-voltage protection (UVP) on the UUT +3.3V, +5V and +12V
- UUT power failure protection (in case OLP or UVP), failure is indicated by red LED per PCI slot
- Backplane is powered from external standard ATX power supply (standard ATX 20/24 pin power connector)
- Meets PCI Bus Specification 2.3 and PCI Express Bus Specifications 1.1
- Supports 3.3V and 5V PCI signals electrical levels (defined via jumpers)
- Supports swapping of all four UUTs without shutting down host computer

3.2 Debugging support

- Allows access to the PCI JTAG interface of each of the four UUTs
- Easy access to PCI logic signals for Logic Analyzer or Oscilloscope through standard header.

3.3 Software

- Hot swapping software for saving and restoring PCI configuration for UUT for hot-swap operation (refer to *eX10 Software Manual for more details*)
- Supported operating systems: Windows, Linux, FreeBSD

4 Installation

4.1 Hardware

Following steps provide the exact sequence that needs to be followed you need to follow in order to properly install the PCI Test Backplane product from AMFELTEC Corp.:

- Turn OFF host computer before installation.
- Remove the chassis cover from host computer.
- Locate an unused PCI express slot and remove the corresponding slot cover from computer chassis.
- Plug-in the x1 PCI express Host Card to selected PCI express slot and attach its bracket to the computer chassis with a screw.
- Put the chassis cover back on the computer.
- Connect the CAT6 cable and flat cable to PCI express Host Card and the other end to the connectors on the PCI Test Backplane.
- Connect the ATX power supply to the PCI Test Backplane.
- Check JP13, JP21 and SW1 setting on the PCI Test Backplane.
- Turn power switch ON for the ATX power supply. LED D5 (STBY) indicates that the standby power is present and that it's ready for operation.
- If jumper JP21 is set in position 2-3 (backplane power will be switched ON/OFF by powering host computer) then you can turn on the host computer (Please check position of the SW1. It has to be in position ON if you need to supply power for the local 4 PCI slots on the backplane).
- If jumper JP21 is set in position 1-2 (backplane power will be controlled by push button S2). Turn backplane power ON by toggling push button S2. Please check position of SW1. It has to be in the ON position if you need to supply power to local 4 PCI slots on the backplane. Then you can turn on the host computer.
- When the system is booted, you can install the software.

NOTE: Recommended to add additional ground connection to the Host PC and to the ATX power supply.

4.2 Software

PCI Test Backplane doesn't require any software/device driver for operation. You will only need to install the software provided by AMFELTLEC Corp. in order to use the hot-swap feature.

Please refer to eX10Suite Manual for software installation details.

5 Operation

5.1 Hot-Swap Support

Perform hot swapping with a certain degree of carefulness. Remember that PCI configuration won't be restored automatically after insertion of a new UUT device unless you use the supplied HOT SWAP software to reload the UUT's PCI configuration.

5.1.1 Remove UUT Device

The following steps describe the sequence for removing UUT device:

1. Save UUT PCI configuration into a file (refer to Software Manual for *more details).*
2. Unload all device drivers associated with the UUT.
3. Set the switch SW1 to "OFF" (disable power).

Now, you can remove UUT device from any of the 4 local PCI slots on the backplane.

5.1.2 Install UUT Device

The following steps describe the sequence for installing UUT device back to the system:

1. Plug in UUT device into original PCI slot on the backplane (If you are using multiple UUT devices, please install these device into original PCI slot positions).
2. Set the switch SW1 to "ON" (enable power).
3. Restore PCI configuration for the UUT device.

Now, the UUT device is ready for use.

6 Hardware Description

6.1 Board Layout

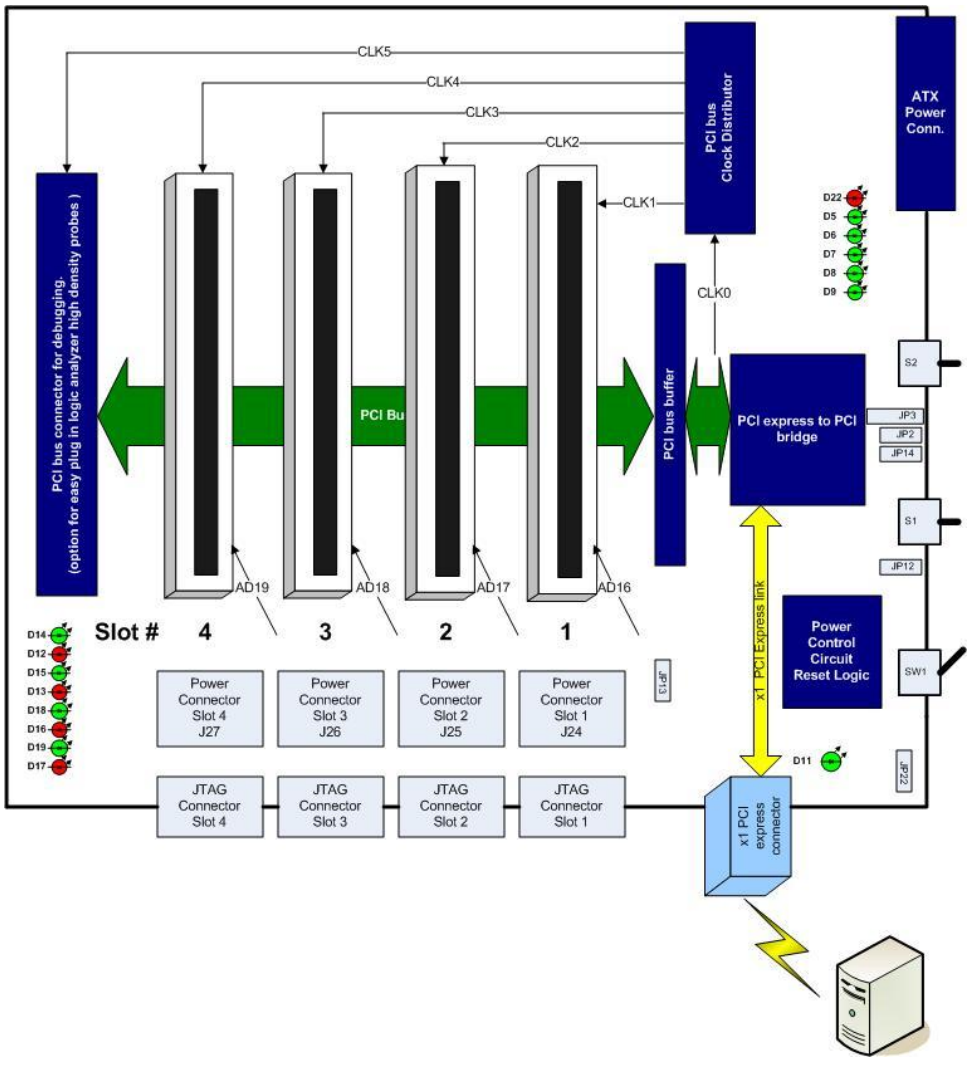

Figure 3: Board layout

6.2 LEDs

Name	Ref. Des.	Color	Usage
LRST	D22	RED	Local RESET signal indicator
STBY	D5	GREEN	Power Supply stand by power indication
5V	D6	GREEN	+ 5V local power on the backplane
3V	D7	GREEN	+ 3.3V local power on the backplane
+12V	D8	GREEN	+ 12V local power on the backplane
-12V	D9	GREEN	- 12V local power on the backplane
LINK	D11	GREEN	PCI express link status indicator
PWR	D14	GREEN	Power status on the slot number 1
FAIL	D12	RED	Power Fail on the slot number 1 (In case overload or under voltage)
PWR	D15	GREEN	Power status on the slot number 2
FAIL	D13	RED	Power Fail on the slot number 2 (In case overload or under voltage)
PWR	D18	GREEN	Power status on the slot number 3
FAIL	D16	RED	Power Fail on the slot number 3 (In case overload or under voltage)
PWR	D19	GREEN	Power status on the slot number 4
FAIL	D17	RED	Power Fail on the slot number 4 (In case overload or under voltage)

Table 1: LEDs

In case that any of "FAIL" LEDs is ON (overload or under voltage condition happens per slot) it is necessarily to toggle local power switch SW1 for reset fail condition.

6.3 Switches

Follow table shows settings for the PCI Test Backplane switches:

Name	Ref. Des.	Type	Usage
BACKPLANE POWER	SW1	Switch	Power switch for all 4 PCI slots. In case OFF state – the power on all 4 PCI slots is off and all PCI signals from the test slots are disconnected from the PCI to PCI express bridge. UUT boards can be replaced. (Hot swap mode).
PWR ON	S2	Push Button	"PWR ON" push button switch ON ATX power supply in case that JP21 in position 1-2 (Local backplane Power supply control).
RESET	S1	Push Button	"RESET" push button provides RESET signal for the local PCI bus.

Table 2: Switches

6.4 Jumpers

Ref. Des.	Type	Usage
JP13	2 pins jumper	Define clock 33 MHz or 66 MHz on the local PCI bus (66MHz if case jumper set).
JP21	3 pins jumper	If 1-2 pins closed, then backplane ATX power supply is controlled by S2 (local control). If 2-3 pins are closed, then backplane ATX power supply is controlled by host computer. (Power On host computer automatically switch power on the test backplane).
JP17,JP18, JP19,JP6	3 pins jumper	Define power source for the PCI VIO signals. If 1-2 pins are closed, then VIO pins will be connected to the 5V power. If 2-3 pins are closed, then VIO pins will be connected to the 3.3V power.

Table 3: Jumpers

6.5 Connectors

Ref. Des.	Type	Usage
JP3	3 pins connector	External Power LED connection (In parallel with D6).
JP2	2 pins connector	External RESET LED connection (In parallel with D22).
JP14	2 pins connector	External RESET push button (In parallel with S1).
JP12	2 pins connector	External Power ON / OFF push button connection (In parallel with S2).
J19,J20, J21,J22	5x2 (2.5 mm) header	JTAG emulator/programmer connection. Direct connection to the "eLoader ™" from AMFELTEC Corp. (per PCI slot).
J24,J25, J26,J27	3 pin connector	Auxiliary Power connector for the UUT board per PCI slot (+.5V, GND, +12V).
J8	2x30 pins header (2.5 mm)	Test connector for all PCI signals for Logic Analyzer connection.
J11,J12, J13,J14	Standard PCI connector	4 PCI connectors (5V key) for the plug in UUT boards (version with 3V key available as a special order).
J7	Standard ATX power supply 24 pin connector	Connector for ATX power supply (Supplies power for PCI Test Backplane).
J10	5x2 (2.5 mm) header	Connector for control cable between PCI Test Backplane and host computer.
J9	RJ45 connector for the PCI express cable connection	Connector for CAT6 cable between PCI Test Backplane and host computer.

Table 4: Connectors

6.6 Power Limits per Slot

Power	Maximum current
+3.3V	4.9A
+5V	4.6A
+12V	0.8A
-12V	0.2A

Table 5: Power Limits

7 Appendix A: JTAG Programming Interface

Function	JTAG connector
TCK	1
N/C	2
TDO	3
VIO (power out)	4
TMS	5
N/C	6
TRST	7
N/C	8
TDI	9
GND	10

Table 6: JTAG connectors J19, J20, J21 and J22

8 Appendix B: Limited warranty

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